REMARKS

The concurrently filed Request for Continued Examination (RCE) Transmittal for the above-identified application is noted. The present amendments constitute the necessary Submission under 37 CFR § 1.114 supporting this RCE Transmittal.

By the present amendments, Applicants are amending claim 103 to recite that the conductive film has a width of 0.18 μm or less; in addition, processing steps for forming second insulating films on side surfaces of the conductive film and for forming second semiconductor regions are set forth between previously recited steps (c) and (d); and claim 103 has been still further amended to recite the removing of the top of the semiconductor substrate to 2.5 nm or less below the surface of the semiconductor substrate by sputter-etching. In view of steps (c)-(f) in presently amended claim 103, the "wherein" clause in previously considered claim 103 has been deleted. Note, for example, paragraph [0021] on page 8 of the Substitute Specification submitted with the Preliminary Amendment filed November 27, 2001. A typographical error has been corrected in claim 110.

In addition, Applicants are adding new claims 113-132 to the application. Claims 113 and 114, each dependent on claim 103, respectively recites that the top of the semiconductor substrate is removed to a depth of 1 nm to 2.5 nm below the surface of the semiconductor substrate; and recites that the top of the semiconductor substrate is removed so as to form a recessed section of the semiconductor substrate. Claims 115 and 116, dependent respectively on claims 111 and 115, respectively recites that the top of the conductive film is recessed by the sputter-etching thereof, and recites the same subject matter expressly set forth in claim 114. Claims 117 and 118, dependent respectively on claims 103 and 117, respectively recites that the depth of the first

semiconductor region is 50 nm or less, and recites that the depth of the second semiconductor region is 150 nm or less. Claims 119 and 120, each dependent on claim 117, respectively recites that the sputter-etching is Ar sputter-etching, and recites that the silicide layers are cobalt silicide layers; and claim 121, dependent on claim 120, recites that the cobalt silicide layers in the surface of the second semiconductor regions have a thickness of 20-40 nm. Claims 122 and 123, dependent respectively on claims 117 and 122, respectively recites that the top of the conductive film is also sputter-etched, to 2.5 nm or less below the surface thereof; and recites that the top of the conductive film is sputter-etched simultaneously with the sputter-etching away the top of the semiconductor substrate.

New independent claim 124 defines a method of fabricating a semiconductor integrated circuit device having a MISFET, including, inter alia, forming a gate electrode of the MISFET having a width of 0.18 μm or less; forming first source/drain regions of the MISFET in the semiconductor substrate self-aligned with the gate electrode, with a depth of the first source/drain regions being 50 nm or less below the surface of the substrate; forming side walls of the MISFET on side surfaces of the gate electrode and forming second source/drain regions of the MISFET, having a greater impurity concentration than that of the first source/drain regions, in the semiconductor substrate self-aligned with the side walls, a depth of the second source-drain regions being 150 nm or less below the surface of the semiconductor substrate; cleaning the surface of the substrate by using hydrofluoric acid as a cleaning agent; removing the top of the second source/drain regions to 2.5 nm or less below the surface of the semiconductor substrate by sputter-etching; depositing a metal layer over at least the gate electrode and first and second source/drain regions, with the removing and the depositing taking

place as sequential processes in the same apparatus; and forming silicide layers by annealing the metal layer. Claims 125 and 126, dependent respectively on claims 124 and 125, respectively recites that the silicide layers are not in contact with the first semiconductor regions; and recites that the silicide layers are positioned such that current leakage between the silicide layers and junctions formed by the first source/drain regions and the semiconductor substrate is prevented.

Independent claim 127 has processing steps corresponding to those in claim 124, but omits the steps of cleaning the surface of the semiconductor substrate by using hydrofluoric acid as a cleaning agent, and deletes recitation of depositing the metal layer, generally reciting forming silicide layers in the surface of the second source/drain regions and the gate electrode; and positively recites that the silicide layers are not in contact with junctions formed by the first source/drain regions and the semiconductor substrate, thereby a current leakage between the silicide layers and the junction is prevented. Claims 128 and 129, each dependent on claim 127, respectively recites that the sputter-etching is Ar sputter-etching, and recites that the silicide layers are cobalt silicide layers, and claim 130, dependent on claim 129, recites that the cobalt silicide layers in the surface of the second semiconductor regions have a thickness of 20-40 nm. Claims 131 and 132, dependent respectively on claims 127 and 131, respectively recites that the top of the gate electrode is also sputter-etched, to 2.5 nm or less below the surface of the gate electrode; and recites that the top of the gate electrode is sputter-etched simultaneously with the sputter-etching away the top of the semiconductor substrate.

It is respectfully submitted that after entry of the present amendments, claims 103 and 105-132 read on the elected species, elected in the Amendment filed February 13, 2004.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the references as applied by the Examiner in rejecting claims in the Office Action mailed May 5, 2004, that is, the teachings of the U.S. Patents to Kamal, et al., No. 6,303,503, and to Zeininger, et al., No. 5,344,793, and European Patent Application No. 325,328, under the provisions of 35 U.S.C. § 102 and 35 U.S.C. § 103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a method of fabricating a semiconductor integrated circuit device as in the present claims, including, inter alia, forming the conductive film (or gate electrode, as in claims 124 and 127) having width of 0.18 μm or less, and forming the specified semiconductor regions, with the method further including removing the top of the semiconductor substrate to 2.5 nm or less below the surface of the semiconductor substrate by sputter-etching, and thereafter forming silicide layers in the surface of the second semiconductor regions and the conductive film (gate electrode in claims 124 and 127). See claim 103; note also claims 124 and 127.

Furthermore, it is respectfully submitted that these references would have neither taught nor would have suggested such method as in the present claims, as discussed previously, and wherein the semiconductor integrated circuit device fabricated has a MISFET, and the steps of removing the top of the second source/drain regions by sputter-etching and depositing the metal layer take place as sequential processes in a

same apparatus (see claim 124); and/or wherein the silicide layers are not in contact with junctions formed by the first source/drain regions and the semiconductor substrate, thereby a leakage current between the silicide layers and the junctions is prevented (see claim 127; note also claims 106 and 126).

In addition, it is respectfully that these references as applied by the Examiner would have neither taught nor would have suggested a method of fabricating a semiconductor integrated circuit device as in the present claims, having features as discussed previously in connection with the independent claims, and furthermore wherein the top of the substrate is removed to a depth of 1 nm to 2.5 nm below the surface of the substrate (see claim 113); or wherein the top of the semiconductor substrate is removed so as to form a recessed section, and/or wherein the top of the conductive film is recessed by the sputter-etching thereof (note claims 114-116).

Moreover, it is respectfully submitted that the teachings of these applied references would have neither taught nor would have suggested the other features of the present invention as in the remaining claims, having features as discussed previously, and furthermore wherein the silicide layers are not in contact with the first semiconductor regions (see claims 105 and 115); and/or wherein the top of the conductive film is also sputter-etched, to 2.5 nm or less below the surface of the conductive film (see claims 111, 122 and 131), particularly wherein the top of the conductive film is sputter-etched simultaneously with the sputter-etching away the top of the semiconductor substrate (see claims 112, 123 and 132); and/or thickness of the cobalt silicide layers as in claims 110 and 121; and/or depths of the various semiconductor regions as in claims 117 and 118.

In any event, even assuming, arguendo, that the teachings of the applied prior art would have established a prima facie case of obviousness, the evidence of record in Applicants' disclosure, and in particular Fig. 9 and the description in connection therewith in paragraphs [0049] – [0051] on pages 20 and 21 of the aforementioned Substitute Specification, together with Figs. 10-13 and the description therewith in paragraph [0054] – [0056] on pages 21-23 of the Substitute Specification, show unexpectedly better results achieved according to the present invention, wherein the sputter-etching etches away only 2.5 nm or less below the surface of the semiconductor substrate, overcomes any prima facie case of obviousness, and clearly establishes patentability of the presently claimed subject matter. In this regard, it is respectfully submitted that this evidence in Applicants' specification must be considered in determining patentability of the present invention. See In re DeBlauwe, 222 USPQ 191 (CAFC 1984).

Note that Applicants have relied on the evidence in their specification, in, for example, in paragraph bridging pages 36 and 37 of the Amendment filed October 20, 2003 but the Examiner has not commented on such evidence. Apparently, the Examiner has ignored this evidence being relied on by Applicants. Clearly, the Examiner must consider this evidence in Applicants' specification and point out any insufficiencies thereof, if the Examiner considers such evidence to be insufficient. However, as can be seen by this evidence in Applicants' specification, it is respectfully submitted that this evidence clearly rebuts any prima facie case of obviousness established by the teachings of the applied references, and clearly supports a conclusion of nonobviousness of the presently claimed subject matter relative to the teachings of the applied references.

The present invention as claimed in the above-identified application is directed to a technique for forming a semiconductor integrated circuit device of increased miniaturization (e.g., with gate electrodes of a width of 0.18 μm or less), particularly effective for application to such a semiconductor integrated circuit device with low levels of current consumption, and especially to devices such as a SRAM (static random access memory).

In forming SRAMs, a silicide layer has been formed on the source/drain regions of MISFETs of the memory, to decrease resistance of the source/drain regions and to decrease the contact resistance between the source/drain and a plug that is subsequently to be formed on the source/drain regions. The silicide layer is formed by depositing a metal layer on the source/drain regions and on the gate electrode, and then causing silicidation in the part where the source/drain regions (silicon substrate) and the metal layer come into contact, and in the part where the gate electrode (silicon layer) and the metal layer come into contact.

However, with the miniaturization that accompanies an increase in the degree of integration of memory cells, gate widths decrease and junction depths of source/drain regions become shallow. Moreover, it is desired to reduce power consumption, particularly in mobile products such as cellular phones and notebook-sized personal computers, which are driven by batteries.

In miniaturized devices, particularly in low power consumption devices, utilizing a conventional technique of forming the silicide wherein approximately 3 nm to 5 nm is etched away from the surface of the silicon substrate and then layers are deposited and thermally processed to form the silicide layer, various problems arise. In particular, formation of a deep layer silicide on the source/drain regions increases current leakage

between the source/drain regions and the semiconductor substrate. As a result, the current when standing by exceeds a critical value, and thus reduces the yield of the products. In addition, even when the standby current is less than a critical value, the time over which it is possible to use a battery-driven mobile product is shortened by the inclusion of a semiconductor integrated circuit device that has a relatively large standby current.

Against this background, Applicants provide a method of fabricating a semiconductor integrated circuit device, for example, that has a standby current of 5 μA or below in tests of operation at 90°C, having improved yield and reduced power consumption; and, in particular, can avoid the aforementioned current leakage. Applicants have found that by sputter-etching away the top of the semiconductor substrate at most 2.5 nm below the surface of the substrate (that is, sputter-etching the semiconductor substrate to a depth of at most 2.5 nm), the aforementioned current leakage can be avoided, and yield improved and power consumption reduced, even in large integration (e.g., a gate electrode having a width of 0.18 μm or less) devices, and with a semiconductor integrated circuit device that has a standby current of 5 μA or below in tests of operation at 90°C.

In addition, by carrying out the etching and metal forming step in the same apparatus, the metal forming step being performed under near-vacuum conditions, the introduction of an oxide film prior to forming the metal film can be avoided.

As for the unexpectedly better advantages achieved with an amount of sputter-etching of 2.5 nm or less, as in the present claims, attention is respectfully directed to Fig. 9 and the description in connection therewith in paragraphs [0049] - [0053] on pages 21 and 22 of Applicants' Substitute Specification. Noting particularly line (b), a

standby current of 5μA or below, it can easily be seen that the yield is improved when the amount of sputter-etching is 1 or 2 nm as compared with the case where no sputter-etching is carried out or where an amount of sputter-etching is 3 or 4 nm. Particularly where the amount of sputter-etching is 3 or 4 nm, the yield becomes lower than in the case where no sputter-etching is carried out, when the critical value of the standby current (Isb) is set to 5 μA or below.

Attention is also respectfully directed to Figs. 10-13 and the corresponding descriptions in connection therewith in paragraphs [0054] - [0056] on pages 22-24 of Applicants' Substitute Specification. As seen particularly in Figs. 11 and 12, as compared with Fig. 13, the greater the amount of sputter-etching, the greater the number of chips with large flows of standby current. As can be appreciated, the smaller the standby current, the better the performance of the chip. Thus, as can be appreciated from the experimental data in Applicants' Substitute Specification, when the amount of sputter-etching is set to 2.5 nm or less, more chips with lower levels of standby current can be obtained, so that more chips with high levels of performance can be obtained. Thus, it is possible to reduce the standby current of the semiconductor integrated circuit device and to reduce its consumption of current. As a result, semiconductor integrated circuit devices formed by the present method are applicable in cellular phones and personal computers which are battery-driven, as they are able to lengthen the times over which these products are used.

Attention is also directed to Fig. 15 of the above-identified application, and the description in connection therewith in paragraph [0064] on pages 25 and 26 of Applicants' Substitute Specification. As is clear therefrom, where the sputter-etching is undesirably great, for example, greater than 2.5 nm, upon forming the silicide the metal

silicide layer approaches the junctions of the source/drain regions, increasing the current leakage. This is avoided according to the present invention; having the sputter-etching to a depth of at most 2.5 nm, such approach to the junction, and resulting increase in the current leakage, can be avoided.

In addition, by etching the surface of the gate electrode by a relatively small thickness, a discontinuity of the layer of metallic silicide can be avoided, so that increase of resistance of the gate electrode layer, and a resulting decrease in operation speed, can be avoided. Note paragraphs [0067] - [0069] on pages 26-28 of Applicants' Substitute Specification. See claims 111, 112, 122, 123, 131 and 132. Simultaneous etching of the top of the substrate and top of the gate electrode facilitates and simplifies the processing. See claims 112, 123 and 132.

European Patent Application No. 325,328 discloses a method of manufacturing a semiconductor device, which includes providing a substrate having doped semiconductor regions for forming at least one electrical component, at least one of the doped regions having an exposed surface area, and depositing metal for forming a metal silicide at the exposed area, with the exposed surface area being subjected to sputter-etching prior to depositing the metal to form the metal silicide. This patent document goes on to disclose that the sputter-etching enables oxide to be removed which would, despite conventional chemical wet etching to remove native oxide during previous processing steps, form on the exposed silicon surface area, and that removal of this oxide facilitates formation of the subsequent silicide. Note column 2, lines 4-22. This patent document also discloses that the sputter-etching also forms a layer of amorphous silicon at each exposed silicon surface area; and thus not only does the sputtering remove oxide which can be detrimental to silicide formation, but the disclosed

method also provides silicon having the same or at least a similar physical structure at each exposed surface area. See column 3, lines 2-10. Note also, column 3, lines 23-26, disclosing ions of an inert gas, preferably argon, being used to sputter-etch the exposed surface areas. Note also from column 6, line 48 to column 7, line 8; column 7, lines 12-16, 26-33 and 39-46; and column 8, lines 7-12. This patent discloses sputter-depositing a layer of refractory metal, of approximately 30-100 nm in thickness. See column 8, lines 12-16. Note also column 9, lines 32-50, emphasizing that the sputter-etching provides an amorphous silicon surface at each exposed surface area so that the metal (e.g., titanium) deposited, is deposited onto the same given type of silicon at each exposed surface, regardless of the type of silicon.

Initially, it is emphasized that according to the method in No. 325,328, the silicon material surface is formed into an amorphous surface. It is respectfully submitted that this disclosure would have neither taught nor would have suggested, and in fact would have taught away from, removing the top of the semiconductor substrate to 2.5 nm or less below the surface of the semiconductor substrate by sputter-etching, as in the present invention, and advantages thereof. It is respectfully suggested that by expressly disclosing formation of an amorphous surface, this would have taught away from removing the substrate surface, by sputter-etching, to the depth as in the present claims.

The contention by the Examiner on page 2 of the Office Action mailed May 5, 2004, that the applied European Patent document teaches, inter alia, argon sputter etching of less than 20 nm (thus encompassing less than 2.5 nm) is noted. However, note that the present claims recite removing the top of the semiconductor substrate by sputter-etching, to 2.5 nm or less below the surface of the semiconductor substrate.

That is, the claims recite much more than argon sputter etching of less than 20 nm, which is how the Examiner has interpreted the teachings of the applied European Patent application. It is respectfully submitted that the teachings of the applied European Patent application would have neither disclosed nor would have suggested the removing by sputter-etching of the semiconductor substrate, much less the level of such removing as in the present claims, and advantages thereof.

The anticipation rejection by the Examiner, on the basis that the reference teaches etching of less than 20 nm (which the Examiner contends thus encompasses less than 2.5 nm) is noted. It is respectfully submitted that such disclosure of etching of less than 20 nm would not have anticipated, within the meaning of 35 U.S.C. § 102, the depth of removal as in the present claims. It is respectfully submitted that the evidence of record establishes unexpectedly better results for removal of a depth of 2.5 nm or less, as compared with removal to a depth of more than 2.5 nm, establishing unexpectedly better results achieved according to the present invention. The level of etching of less than 20 nm, while encompassing less than 2.5 nm, does not anticipate, within the meaning of 35 U.S.C. § 102, less than 2.5 nm, just like a range of 1-100 does not anticipate (within the meaning of 35 U.S.C. § 102) a range of 50-60.

It is respectfully submitted that the additional teachings of Zeininger, et al., would not have rectified the deficiencies of No. 325,328, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Zeininger, et al. discloses a method of forming silicided junctions of semiconductor integrated circuit devices, wherein a silicon wafer is first precleaned with hydrofluoric acid; and thereafter, the silicon wafer is transferred to a conventional cobalt sputtering tool where it is sputter cleaned with bombardment with low energy ions. The

low energy bombardment forms an ultra-shallow damage region in the bulk silicon; and, thereafter, cobalt metal is deposited on the silicon wafer at room temperature so as to form the $CoSi_2$ layer. Note the paragraph bridging columns 1 and 2 of this patent. See also column 2, lines 58-64.

Initially, it is noted that Zeininger, et al. discloses sputter cleaning, not sputter etching. It is respectfully submitted that one of ordinary skill in the art as described in No. 325,328, would not have looked to the sputter cleaning of Zeininger, et al.

In any event, even assuming, arguendo, that the teachings of No. 325,328 and Zeininger, et al. were properly combinable, such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including removing the silicon substrate to depths as in the present claims, and unexpectedly better advantages achieved thereby, as discussed in the foregoing.

It is emphasized that all of the claims being presently considered on the merits recite a conductive film width (or gate electrode width) of 0.18 μm or less. It is respectfully submitted that such devices have reduced size (increased integration). However, with devices having gate electrode widths as in the present claims, the leakage current problem is extremely acute and, in essence, is a new problem as compared with conventional structures. This new problem is solved by controlling the etch removal of the silicon substrate at levels as in the present claims. It is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested this new problem arising in connection with devices having decreased gate electrode widths (e.g., gate electrode widths of 0.18 μm or less), and would have neither disclosed nor would have suggested the solution to this problem as

achieved by the present invention, having removal of the substrate to a maximum depth as in the present claims.

It is respectfully submitted that the combined teachings of No. 325,328, Kamal, et al. and Zeininger, et al. would have neither disclosed nor would have suggested the present invention.

No. 325,328 and Zeininger, et al. have been previously discussed.

Kamal, et al. discloses processes for the formation of cobalt salicide layers during semiconductor device fabrication, including a sputter etched surface preparation step prior to the cobalt layer deposition step. This patent discloses that after providing the MOS transistor structure that includes source and drain regions disposed in the silicon substrate on either side of the silicon gate, the surface of the transistor structure is then prepared using an argon sputter etch process with DC bias of less than –280 volt, the argon sputter etch processing conditions being optimized in order to minimize the back sputtering of silicon onto the gate side wall spacers while still adequately removing native silicon dioxide from the source region, drain region and silicon gate. Note column 1, lines 9-13; and columns 2, lines 48-66. This patent discloses that following the argon sputter etch processing step, a cobalt layer is deposited on the source region, drain region, silicon gate and gate side wall spacers. See column 3, lines 9-11. Note also column 5, lines 60-65, for disclosure of the argon sputter etch; this patent discloses that such etch is to remove native silicon dioxide, with native silicon dioxide removal targets of between 20 and 60 angstroms.

Even assuming, arguendo, that the teachings of Kamal, et al. and Zeininger, et al. were properly combinable with the teachings of No. 325, 328, it is respectfully submitted that these teachings would have neither disclosed nor would have suggested

the invention in the claims presently being considered on the merits, including the gate electrode having the recited width and problems arising in connection with miniaturized structure, as discussed previously; and avoiding leakage current by removing the top of the semiconductor substrate to 2.5 nm or less below the surface of the substrate by sputter-etching; and, moreover, these references would have neither disclosed nor would have suggested the other features of the present invention as discussed in the foregoing, and advantages thereof.

The Request For Interview Prior To A Further Office Action in the above-identified application, filed concurrently herewith, is noted. The Examiner is respectfully requested to contact the undersigned to schedule such an interview, at the convenience of the Examiner, prior to a further Office Action on the merits in the above-identified application, in order to resolve any outstanding issues.

Further examination of the above-identified application in due course, and ultimate allowance of claims being considered on the merits herein, are respectfully requested.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of

this paper, including extension of time fees, to the Antonelli, Terry, Stout & Krause, LLP Deposit Account No. 01-2135 (Docket No. 501.40724X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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